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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,447	11/06/2003	Takashi Hotta	501.25958CV7	7625

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EXAMINER	
BUTLER, DENNIS	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,447	HOTTA ET AL.	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/184,782.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11062003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on November 6, 2003. Claims 1-6 are pending.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-6 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 15, 20, 25, 30, 31 and 37 of U.S. Patent No. 5,133,064. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention including a phase locked loop (clock generating means/clock generator, phase comparator, low pass filter, voltage controlled oscillator, frequency divider and feedback path) and a logic device that is described at column 9, lines 51-57 as comprising a memory. The PLL and logic device being formed on a single semiconductor substrate. The claims in the patent do not explicitly recite the interface circuit. However, interface

circuits are a common component of both logic devices and memory devices that allow data to be input to the device and output from the device and it would have been obvious to include an interface circuit on a semiconductor substrate that includes a logic device or a memory device.

4. Claims 1-6 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 4, 5 and 9 of U.S. Patent No. 6,675,311. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention including a phase locked loop (clock generating means/clock generator) and a logic device that is described at column 9, lines 36-42 as comprising a memory. The PLL and logic device being formed on a single semiconductor substrate. The claims in the patent do not explicitly recite the interface circuit. However, interface circuits are a common component of both logic devices and memory devices that allow data to be input to the device and output from the device and it would have been obvious to include an interface circuit on a semiconductor substrate that includes a logic device or a memory device.

5. Claims 1-6 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 5,974,560. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention including a phase locked loop, a logic device that is described at column 9, lines 28-34 as comprising a memory and an interface circuit. The PLL, interface circuit and logic device

being formed on a single semiconductor substrate. Claims 6-10 of the patent do not explicitly recite the interface circuit. However, interface circuits are a common component of both logic devices and memory devices that allow data to be input to the device and output from the device and it would have been obvious to include an interface circuit on a semiconductor substrate that includes a logic device or a memory device.

6. Claims 1-6 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 5,542,083. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention including a phase locked loop, a logic device that is described at column 9, lines 36-42 as comprising a memory and an interface. The PLL, interface and logic device being formed on a single semiconductor substrate. The claims in the patent recite a plurality of units while the claims of the present application recite a single unit. However, it would have been obvious to apply the claimed invention to a plurality of units because the recited interface circuit of the application is for outputting data from the unit and the memory inputs an address. Therefore, the claimed invention of the application is designed to communicate with other units.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talbot, U. S. Patent 4,689,581 in view of Inmos Limited, European Patent Application 0 113 516.

Per claims 1, 3 and 5:

A) Talbot teaches the following claimed items:

1. a memory apparatus formed on one semiconductor substrate with figure 1, at column 1, lines 39-60, at column 2, lines 47-57 and at column 10, lines 44-46;

2. a PLL circuit generating a second clock signal with PLL 4 of figure 1, at column 3, lines 5-65 and at column 10, lines 30-43;

3. an interface circuit with Pins 3 of figure 1 and the related input/output circuitry and at column 2, lines 43-63.

B) The claims differ from Talbot in that Talbot fails to explicitly teach the memory part/RAM/ROM as claimed.

C) However, Talbot describes that logic device 2 of figure 1 can be any circuit capable of performing logic operations including the microcomputer described in European Application 83307078.2 (Publication 0 113 516) at column 2, lines 47-57 and at column 10, lines 44-46. Therefore, Talbot discloses the claimed invention except for explicitly describing the memory part/RAM/ROM. Inmos Limited teaches that it is known to include a memory part/RAM/ROM as a logic device as set forth with figures 1-3, at page 7, last paragraph and at pages 9-10. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a memory part/RAM/ROM as a logic device, as taught by Inmos Limited, in order to provide for storage of programs and data in a data processing system. One of ordinary skill in the art would have been motivated to combine Talbot and Inmos Limited because of Talbot's suggestion that logic device 2 could be Inmos Limited's microcomputer at column 2, lines 47-52.

Per claims 2, 4 and 6:

Inmos Limited describes the memory part/RAM/ROM inputs an address responsive to a clock with figures 6-7 and 15-16 and at pages 10-13 and 44. In addition, as described in the above rejection, Talbot describes generating a second clock signal for the logic device of Inmos Limited at column 1, lines 39-60 and at column 2, lines 47-57.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax number for this unit is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler
Dennis M. Butler
Primary Examiner
Art Unit 2115